MT7921LEN Product Brief

802.11a/b/g/n/ac/ax Wi-Fi 2T2R + Bluetooth v5.2 Combo Chip

System overview

1.1　General Description

MT7921 is highly integrated single chip which features a low power 2x2 11a/b/g/n/ac/ax dual-band Wi-Fi subsystem and a Bluetooth subsystem. The Wi-Fi subsystem contains the 802.11a/b/g/n/ac/ax radio, baseband, and MAC that are designed to meet both the low power and high throughput application, and 32-bit RISC MCU to handle Wi-Fi tasks. The Bluetooth subsystem contains the Bluetooth radio, baseband, link controller, and 32-bit RISC MCU for Bluetooth protocols.

1.2　Features

1.2.1　Technology and package

- MT7921 – DRQFN 11.5x8.7 109 pins package

1.2.2　Power management and clock source

- Integrate high efficiency power management unit with single 3.3V power supply input
- Support 40MHz crystal clock with low power operation in idle mode

1.2.3　Platform

- 32-bit RISC MCU for Wi-Fi/Bluetooth protocols
- Embedded SRAM/ROM
- UART interface with hardware flow control
- Programmable and multiplexed GPIO pins
- Host interface: PCIe device fully compliant to PCIe v2.1 specification

1.2.4　WLAN

- IEEE 802.11 a/b/g/n/ac/ax compliant
- Support 20MHz/40MHz bandwidth in 2.4GHz band and 20/40/80M bandwidth in 5GHz band
- MT7921 supports MU-MIMO RX and DBDC (dual band dual concurrent)
- MT7920 supports MU-MIMO RX
- Support STBC, LDPC, TX Beamformer and RX Beamformee
- Greenfield, mixed mode, legacy modes support
- IEEE 802.11 d/e/h/i/j/k/mc/r/v/w support

- Security support for WFA WPA/WPA2 personal, WPS2.0, WAPI
- QoS support of WFA WMM, WMM PS
- Integrated LNA, PA, and T/R switch
- Optional external LNA and PA support.

1.2.5   Bluetooth

- Bluetooth specification 2.1+EDR
- Bluetooth 4.2 Low Energy (LE)
- Bluetooth 5.2
- Support BLE Isochronous channel + NBC
- Integrated BALUN and PA
- Scatternet support: Up to 7 piconets simultaneously with background inquiry/page scan
- Up to 7 BT link + 16 BLE link
- Support SCO and eSCO link with re-transmission
- Support wide-band speech and hardware accelerated SBC codec for A2DP streaming
- Packet loss concealment
- Channel quality driven data rate adaptation
- Channel assessment and WB RSSI for AFH

1.2.6   Miscellaneous

- Integrate efuse to store device specific information and RF calibration data.
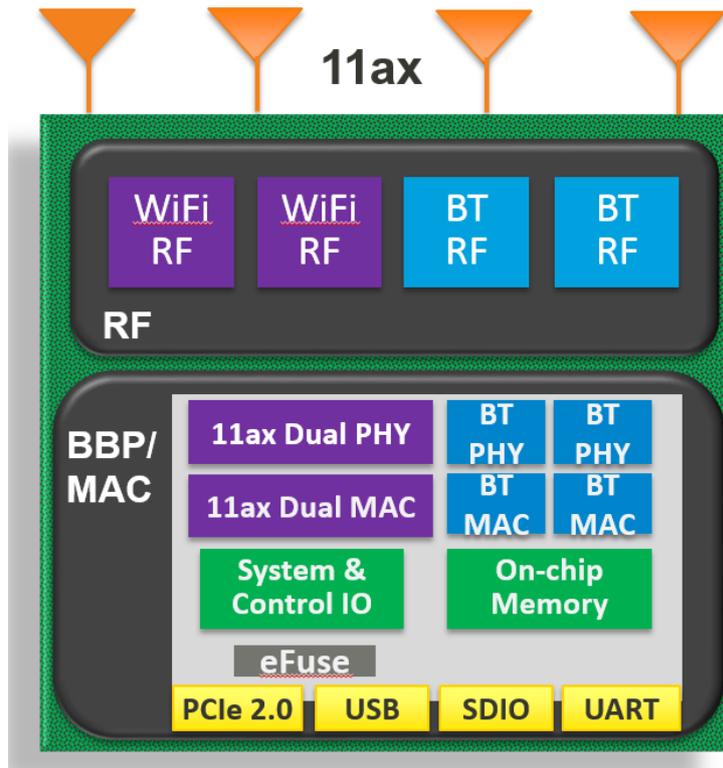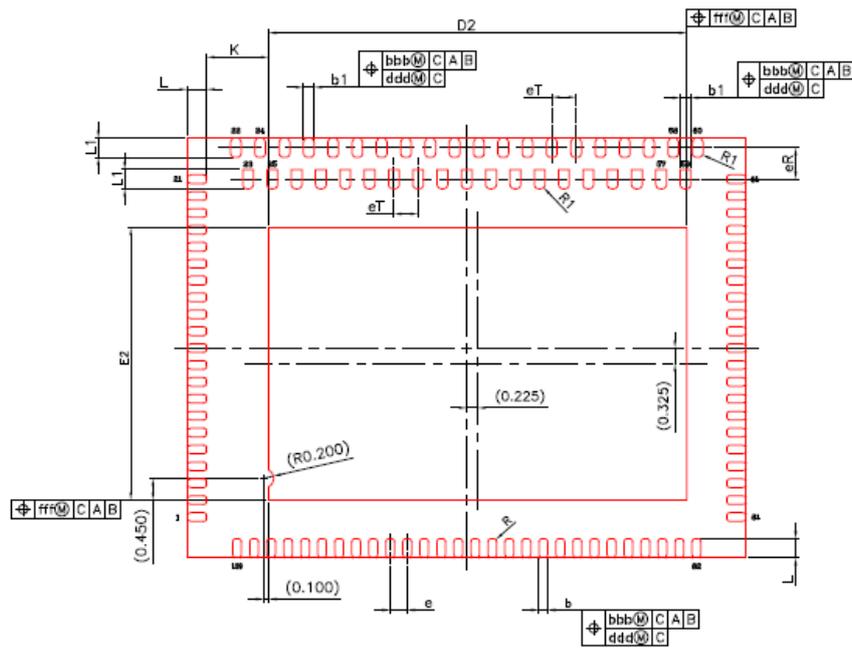- Advanced FDD/TDD mode Wi-Fi/Bluetooth coexistence scheme

1.3 Block Diagram

Figure 1 MT7921 system-on-chip block diagram

Package Specification

2.1 Pin Payout

MT7921LEN

Top side (pins 109–82, left to right):

Pin	Name	Pin	Name	Pin	Name
109	MLDO_VOUT	100	GPIO14	91	TSTRST_B
108	HIFLDO_VOUT	99	GPIO15	90	RFIO_BT
107	ALDO18	98	DVDDIO	89	ISO_BT
106	AVDD33_MISC	97	DVDDM	88	AVDD33_PA_BT
105	PMU_EN	96	DVDD	87	AVDD12_HF_BT
104	PHYLDO18	95	DVDD	86	AVDD18_BT
103	VREF	94	DVDD	85	AVDD12_BT_MISC
102	DVDDIO_18V	93	AVDD12_WF0_AFE	84	GND
101	GPIO13	92	GPIO16	83	GND
				82	GND

Left side (pins 1–21):

Pin	Name
1	AVDD12_LDO
2	CLDO_VOUT
3	CLDO_VOUT_S / VO_FB_BUCKD
4	VO_FB_BUCKR
5	AVDD33_BUCKR
6	LX_BUCKR
7	AVSS33_BUCKR
8	AVSS33_BUCKD
9	LX_BUCKD
10	AVDD33_BUCKD
11	DVDDM
12	DVDD
13	DVDD
14	DVDD
15	DVDDIO
16	GPIO12
17	GPIO11
18	GPIO10
19	GPIO9
20	GPIO8
21	GPIO7

Right side (pins 81–61):

Pin	Name
81	AVDD12_WF0_TRX
80	AVDD18_WF0_TOP
79	AVDD33_WF0_A_TX
78	GND
77	WF0_A_RFIO
76	AVDD33_WF0_A_PA
75	WF0_RXA_AUX_IN
74	WF0_RXG_AUX_IN
73	AVDD33_WF0_G_PA
72	WF0_G_RFIO
71	GND
70	AVDD33_WF1_A_TX
69	AVDD18_WF1_A_TRX
68	PAD_WF1_A_RFIO
67	AVDD33_WF1_A_PA
66	WF1_RXA_AUX_IN
65	WF1_RXG_AUX_IN
64	AVDD33_WF1_G_PA
63	WF1_G_RFIO
62	GND
61	AVDD33_WF1_G_TX

Bottom side (pins 22–60, left to right):

Pin	Name	Pin	Name	Pin	Name
22	GPIO6	35	USB_DM	48	NC
23	PCIE_CKP	36	DVDDM	49	XO_IP
24	PCIE_CKN	37	DVDD	50	XO_IN
25	AVDD18_PCIE	38	DVDDIO	51	GND
26	PCIE_TXP	39	GPIO5	52	AVDD12_XO
27	AVDD09_PCIE	40	GPIO4	53	AVDD12_WF1_AF
28	PCIE_TXM	41	GPIO3	54	AVDD18_XO
29	GND	42	GPIO2	55	AVDD12_WF1_TR
30	PCIE_RXN	43	AVDD12_AFE	56	AVDD18_WF1_TOP
31	AVDD18_USB	44	GPIO1	57	A_GPIO0
32	PCIE_RXP	45	AVDD18_AFE	58	A_GPIO1
33	AVDD33_USB	46	GPIO0	59	A_GPIO3
34	USB_DP	47	GND	60	A_GPIO2

2.2 Package Information

2X — aaa C A

D → A

B

PIN#1 IDENTIFY:
Laser Mark

E

2X — aaa C B

TOP VIEW

(0.075)

A2 // ccc C

— eee C

A

SEATING PLANE

A1   A3

C

SIDE VIEW

BOTTOM VIEW

Item		Symbol	MIN.	NOM.	MAX.
Total height		A	0.80	0.85	0.90
Stand off		A1	0.00	0.02	0.05
Mold thickness		A2	0.65	0.70	0.75
Lead frame thickness		A3	0.15 REF.		
Lead width		b	0.13	0.18	0.23
Lead width		b1	0.18	0.22	0.30
Package size	X	D	11.40	11.50	11.60
	Y	E	8.60	8.70	8.80
E-PAD size	X	D2	8.50	8.60	8.70
	Y	E2	5.55	5.65	5.75
Lead length		L	0.30	0.40	0.50
Lead length		L1	0.30	0.40	0.50
Lead pitch		e	0.35 bsc		
Lead pitch		eT	0.50 bsc		
Lead pitch		eR	0.65 bsc		
Lead arc		R	0.065	---	---
Lead arc		R1	0.09	---	0.14
Lead to E-PAD tolerance		K	0.20	---	---
Package tolerance		aaa	0.10		
Package profile of a surface		bbb	0.10		
Lead profile of a surface		ccc	0.10		
Lead position		ddd	0.05		
Lead profile of a surface		eee	0.08		
Epad position		fff	0.10		

2.3 Ordering Information

Part number	Package	Operational temperature range
MT7921LEN	11.5mm x 8.7mm 109pin DRQFN	-10~70°C

2.4 Top Marking

MEDIATEK
MT7921LEN
DDDD-####
BBBBBBB
BBBBBBB

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MT7921LEN : Part number
DDDD      : Date code
####      : Internal control code
BBBBBBB   : Lot number
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